REMARKS

This paper is being provided in response to the Final Office Action mailed October 7, 2004, for the above-referenced application. Applicants note that claims 1-19 and 29 have been previously cancelled without prejudice or disclaimer of the subject matter thereof. In this response, Applicants have amended claims 20, 23, 24 and 28 and added new claims 30-36 to clarify that which Applicants consider to be the invention. Applicants respectfully submit that the amendments to the claims and the new claims are fully supported by the originally-filed specification.

The rejection of claims 20-27 under 35 U.S.C. 102(e) as being anticipated by U.S. Patent No. 6,395,632 to Farrar (hereinafter "Farrar") and the rejection of claim 28 under 35 U.S.C. 102(e) as being anticipated by Farrar or in the alternative under 35 U.S.C. 103(a) as being obvious over Farrar is hereby traversed and reconsideration is respectfully requested in view of the amendments to the claims contained herein.

Independent claim 20, as amended herein, recites a semiconductor device. An organic film having low dielectric constant and including no silicon is formed on a semiconductor substrate. At least two silicon included organic films are formed on lower and upper surfaces of the organic film having low dielectric constant, wherein a first silicon included organic film is formed on the lower surface facing the semiconductor substrate and a second silicon included organic film is formed on the upper surface. Further, the second silicon included organic film is larger in thickness than the first silicon included organic film. Claims 21 and 22 depend on independent claim 20.

Independent claim 23, as amended herein, recites a semiconductor device. The device includes at least two silicon included organic films composed of a first organic compound including silicon. A silicon non-included organic film composed of a second organic compound including substantially no silicon is disposed between the silicon included organic films. The silicon non-included organic film has an upper surface and a lower surface facing a substrate, wherein the silicon included organic film disposed on the upper surface is larger in thickness than the silicon included organic film disposed on the lower surface. Claims 25-27 depend on independent claim 23.

Independent claim 24, as amended herein, recites a semiconductor device. A first silicon included organic film is formed on an upper side of a substrate and is composed of a first organic compound including silicon. A silicon non-included organic film is formed on an upper side of the first silicon included organic film and is composed of a second organic compound including substantially no silicon. A second silicon included organic film is formed on an upper side of the silicon non-included organic film. A lower wiring trench is formed through said second silicon included organic film, said silicon non-included organic film and down to and through said first silicon included organic film. A conductor is formed within the lower wiring trench.

Independent claim 28, as amended herein, recites a semiconductor device. The device includes an organic film composed of an organic compound including no silicon. A hard mark is included for use in etching an organic film composed of an organic compound including no silicon, the hard mask including a first organic compound including silicon. The device further

includes an etching stopper film for use in etching the organic film composed of the organic compound including no silicon, the etching stopper film including a second organic compounding including silicon. The hard mask is disposed on an upper surface of the organic film composed of an organic compound including no silicon and the etching stopper film is disposed on a lower surface of said organic film, wherein the hard mask is larger in thickness than said etching stopper film.

The Farrar reference discloses an interconnect structure with a plurality of low dielectric constant insulating layers acting as etch stops. Figures 16-23 of Farrar illustrates a substrate layer 50 on which is formed an organic layer 55 on which is further formed up to three layers, preferably organic SILK or inorganic NANOGLASS layers (57, 57a and 55a). (See col. 4, lines 59-63 and col. 6, beginning line 50 of Farrar.)

Applicants' independent claims 20, 23 and 28, as amended herein, all recite at least the features of a semiconductor device including *an organic film having low dielectric constant and including no silicon* and *at least two silicon included organic films formed on lower and upper surfaces of the organic film having low dielectric constant, wherein a first silicon included organic film is formed on said lower surface facing the semiconductor substrate and a second silicon included organic film is formed on said upper surface, and wherein said second silicon included organic film is larger in thickness than said first silicon included organic film.* Applicants have found that a semiconductor device having this structure enables one of the silicon included organic films to function as an etching stop layer and the other of the silicon included organic films to function as a hard mask, thereby offering improved manufacturing

capability. As a result of this structure, interlayer capacitance can be beneficially reduced in a semiconductor device thus manufactured. (See page 38, lines 3-12 and beginning page 40, line 9 of the present application.) Further, to take advantage of the improved manufacturing capability during the etching processes, it is desirable that the second included organic film be larger in thickness than the first silicon included organic film, and thereby capable of functioning as a cap film on a lower wiring structure, such that etching steps may be combined without the necessity of using additional photo resist layers, etching stop layers or other layers during etching. (See page 42, lines 2-11 and particularly Figs. 8(a)-(c) and 9(a)-(b) of the present application.)

Applicants respectfully submit that the Farrar reference does not teach or fairly suggest at least the above-noted features as claimed by Applicants. Farrar discloses insulating films utilized as etch stops including a layer 55 disposed on a substrate on which is further disposed other organic and inorganic layers, preferably including organic SILK layers or inorganic NANOGLASS layers but also potentially including BCB layers (57, 57a, 55a). (See, for example, col. 5, lines 31-58 and Figure 17 of Farrar.) Farrar does not appear to recognize the advantages, as found by Applicant and recited in the present claimed invention, of specifically designing a semiconductor device with a layer structure that improves manufacturing efficiency that results from an organic film having a low dielectric constant and including no silicon and disposed between at least two silicon included organic films, as discussed below.

Specifically, Farrar does not disclose that the silicon included organic film disposed on an upper surface of the organic film is larger in thickness than the silicon included organic film disposed on a lower surface of the organic film facing the substrate. As described in detail (for

purposes of example only) in Figures 8 and 9 and beginning on page 40, line 9 of the present application, Applicants disclose an embodiment of the invention involving etching procedures with N2/H2 plasma and N2/O2 plasma and the corresponding results with respect to the SILK films and BCB films. In particular, Applicants have found that it is desirable that the second silicon included organic film (BCB) film is formed to be larger in thickness than the first BCB film and which results in the combined and efficient use of etching processes without the utilization of additional photo resist layers and other layers during etching. (See page 42, lines 6-11 of the present application). Farrar does not disclose any such respective thicknesses in the disclosed layer structures, nor does Farrar disclose with particularity the materials of the layer structure as is recited by Applicant to achieve Applicant's stated advantages, and it is not possible to glean this information from Farrar's non-scaled figures.

Accordingly, Applicants submit that nothing in Farrar teaches or fairly suggests at least the above-noted features as claimed by Applicants. In view of the above, Applicants respectfully request that this rejection be reconsidered and withdrawn.

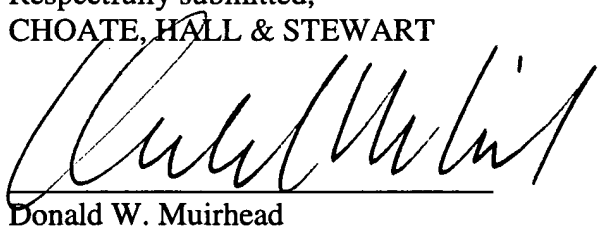
Furthermore, with respect to claim 24, Applicants recite features of a semiconductor device that includes a *lower wiring trench formed through said second silicon included organic film, said silicon non-included organic film and down to and through said first silicon included organic film.* The recited wiring trench is made possible as a result of the three layer structure of the silicon included organic films and the silicon non-included organic films, such that the etching process permits the wiring structure to extend down to the first silicon included organic film while maintaining the second silicon included organic film disposed on the upper surface of

the silicon non-included organic film. Farrar does not arguably disclose a wiring trench that extends through the specified material layers, as claimed by Applicants. Each of the individually formed trenches disclosed by Farrar extends into only two layers (see, for example, Figures 16-22 of Farrar.) Accordingly, in view of the above, Applicants respectfully request that the rejection of this claim be reconsidered and withdrawn.

Further, Applicants have added new claims 30-36 and respectfully submit that these claims are allowable over the prior art of record.

Based on the above, Applicant respectfully requests that the Examiner reconsider and withdraw all outstanding rejections and objections. Favorable consideration and allowance are earnestly solicited. Should there be any questions after reviewing this paper, the Examiner is invited to contact the undersigned at 617-248-4038.

Respectfully submitted,
CHOATE, HALL & STEWART



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